ABSTRACT OF THE INVENTION

An MOS device comprising a gate dielectric formed on a first conductivity type region. A gate electrode formed on the gate dielectric. A pair of sidewall spacers are formed along laterally opposite sidewalls of the gate electrode. A pair of deposited silicon or silicon alloy source/drain regions are formed in the first conductivity region and on opposite sides of a gate electrode wherein the silicon or silicon alloy source/drain regions extend beneath the gate electrode and to define a channel region beneath the gate electrode in the first conductivity type region wherein the channel region directly beneath the gate electrode is larger than the channel region deeper into said first conductivity type region.